CLAIMS

1. A body diode comparator circuit for a synchronous rectified FET driver, wherein the driver is responsive to a PWM signal and has a phase node coupled between upper and lower switching FETs, and wherein the PWM signal has first and second phases for each PWM cycle, said body diode comparator circuit comprising:

   a sample circuit for sampling an initial voltage of the phase node during the first phase of the PWM signal and for providing a sum voltage indicative of said initial voltage added to the voltage level of the phase node during the second phase of the PWM signal; and

   a comparator that compares said sum voltage with a predetermined reference voltage and that provides an output indicative of an activation state of the lower FET during the second phase of the PWM signal.

2. The body diode comparator circuit of claim 1, further comprising:

   said comparator having first and second inputs;

   a first voltage source providing said predetermined reference voltage;

a switch circuit that samples said predetermined reference voltage during the first phase of the PWM signal and that applies a first voltage indicative of said predetermined reference voltage to said first input of said comparator during the second phase of the PWM signal; and

said sample circuit being operative to sample a second voltage indicative of said initial voltage of the phase node during the first phase of the PWM signal, to determine said sum voltage by adding said second voltage to the voltage level of the phase node during the second phase of the PWM signal, and to apply said sum voltage to said second input of said comparator.

3. The body diode comparator circuit of claim 1, further comprising:

said comparator having first and second inputs;

a first voltage source providing said predetermined reference voltage;

a second voltage source providing a common mode voltage;

a switch circuit that stores a first difference voltage between said predetermined reference voltage and said common mode voltage during the first phase of the PWM signal and that applies said first difference voltage to said first input of said comparator during the second phase of the PWM signal; and

said sample circuit being operative to store a second difference voltage between said common mode voltage and said initial voltage of the phase node during the first phase of the PWM signal and to provide a sum of the phase node voltage and said second difference voltage to said second input of said comparator during the second phase of the PWM signal.

4. The body diode comparator circuit of claim 3, wherein:

said switch circuit comprises:

a first capacitor coupled between said first input of said comparator and a first node;

a first switch coupled between said second voltage source and said first input of said comparator;

a second switch coupled between said first voltage source and said first node; and

a third switch coupled between said first node and ground;

wherein said sample circuit comprises:

a second capacitor coupled between said second input of said comparator and the phase node; and

a fourth switch coupled between said second voltage source and said second input of said comparator; and

wherein said first, second and fourth switches are open during the first phase and closed during the second phase of the PWM signal and wherein said third switch is closed during the first phase and open during the second phase of the PWM signal.

5. The body diode comparator circuit of claim 4, further comprising a voltage limiter coupled between the phase node and said second capacitor.

6. The body diode comparator circuit of claim 1, wherein said comparator includes a blanking circuit.

7. A rectified synchronous FET power regulator, comprising:

an upper FET and a lower FET coupled together at a phase node and coupled between an input voltage signal and a reference terminal of a voltage source;

PWM logic that switches said upper and lower FETs based on a PWM signal having first and second states; and

a comparator circuit, coupled to said phase node and said PWM logic, that detects activation state of said lower FET, said comparator circuit comprising:

a sample circuit that samples an initial voltage of said phase node during said first state of said PWM signal and that provides a sum voltage indicative of a sum of said initial voltage and the voltage level of said phase node during said second state of said PWM signal; and

a comparator that compares said sum voltage with a predetermined reference voltage and that provides an output indicative of said activation state of said lower FET.

8. The rectified synchronous FET power regulator of claim 7, wherein said upper and lower FETs comprise MOSFETs.

9. The rectified synchronous FET power regulator of claim 7, wherein said comparator circuit further comprises:

said comparator having first and second inputs;

a first voltage source providing said predetermined reference voltage;

a switch circuit that samples said predetermined reference voltage during said first state of said PWM signal and that applies a first voltage indicative of said predetermined reference voltage to said first input of said comparator during said second state of said PWM signal; and

said sample circuit being operative to sample a second voltage indicative of said initial voltage of the phase node during said first state of said PWM signal, to determine said sum voltage by adding said second voltage to the voltage level of the phase node during said second state of said PWM signal, and to apply said sum voltage to said second input of said comparator.

10. The rectified synchronous FET power regulator of claim 7, wherein said comparator circuit further comprises:

said comparator having a non-inverting and an inverting input;

a first voltage source providing said predetermined reference voltage;

a second voltage source providing a common mode voltage;

a switch circuit that stores a first difference voltage between said predetermined reference voltage and said common mode voltage during said first state of said PWM signal and that provides said first difference voltage to said non-inverting input of said comparator during said second state of said PWM signal; and

said sample circuit being operative to store a second difference voltage between said common mode voltage and said initial voltage of said phase node during said first state of said PWM signal, to add said second difference voltage to said phase node voltage to determine said sum voltage, and to provided said sum voltage to said inverting input of said comparator.

11. The rectified synchronous FET power regulator of claim 10, wherein:

said switch circuit comprises:

a first capacitor coupled between said non-inverting input of said comparator and a first node;

a first switch coupled between said second voltage source and said non-inverting input of said comparator;

a second switch coupled between said first voltage source and said first node; and

a third switch coupled between said first node and said reference terminal of said voltage source;

wherein said sample circuit comprises:

a second capacitor coupled between said inverting input of said comparator and said phase node; and

a fourth switch coupled between said second voltage source and said inverting input of said comparator; and

wherein said first, second and fourth switches are open during said first state and closed during said second state of said PWM signal and wherein said third switch is closed during said first state and open during said second state of said PWM signal.

12. The rectified synchronous FET power regulator of claim 11, further comprising a voltage limiter coupled between said phase node and said second capacitor.

13. The rectified synchronous FET power regulator of claim 7, wherein said comparator includes a blanking circuit.

14. A method of detecting the activation state of a lower switching FET of a synchronous rectified FET driver which toggles activation of upper and lower switching FETS coupled together at a phase node, said method comprising:

storing a first voltage level indicative of the initial voltage level of the phase node while the lower FET is turned on; and

determining when the voltage level of the phase node falls below the initial voltage level by a predetermined amount after the FET driver initiates turning off the lower FET.

15. The method of claim 14, wherein said determining comprises comparing a predetermined reference voltage with the first voltage level added to the voltage level of the phase node.

16. The method of claim 14, further comprising:

said storing a first voltage level indicative of the initial voltage level comprising storing a first voltage difference between a common mode voltage and the initial voltage level;

storing a second voltage difference between the common mode voltage and a predetermined reference voltage level; and

said determining comprising comparing the second voltage difference with a sum of the first voltage difference and the voltage level of the phase node.

17. The method of claim 16, wherein said storing a first voltage difference comprises charging a first capacitor having a first end coupled to the phase node and a second end coupled to a common mode voltage source, and wherein said storing a second voltage difference comprises charging a second capacitor having a first end coupled to a reference voltage source and a second end coupled to the common mode voltage source.

18. The method of claim 17, wherein said comparing comprises, after the FET driver initiates turning off the lower FET, switching the second end of the first capacitor to a first input of a comparator, switching the first end of the second capacitor to ground, and switching the second end of the second capacitor to a second input of the comparator.

19. The method of claim 14, further comprising ignoring initial ringing of the phase node immediately after the FET driver initiates turning off the lower FET.

20. The method of claim 14, further comprising turning on the upper FET after the FET driver initiates turning off the lower FET and when the voltage of the phase node falls below the initial voltage level by the predetermined amount.